A Monolithic 16-Channel Analog Array Normalizer

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A Monolithic 16-Channel Analog Array Normalizer

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Abstract—A monolithic circuit has been developed which accepts 16 parallel voltage inputs having peak values which may be as small as 15 mV or as large as 15 V, and generates 16 concurrent output voltages which are in the same ratios as the inputs with a peak amplitude controllable by the user. Response time is in the region of 1 μs at full scale. The chip includes provisions for expansion to any number of channels. Operation is from supplies of ±3 to 15 V at a quiescent current of 125 μA. Details of the design principles and peripheral circuitry are provided. Measurements of static accuracy and dynamic performance demonstrate that this approach may often simplify preprocessing of signal arrays in pattern-recognition applications.

BACKGROUND AND MOTIVATION

DIGITAL array processors are widely used to minimize the execution time of multivariable algorithms. However, the internal procedures are still intrinsically *serial.* Truly concurrent signal processing remains, for the present, the province of analog circuits. The monolithic circuit described here performs *concurrent amplitude normalization* on an input array of 16 unipolar voltage inputs. The resulting output is an array of 16 unipolar voltages, the largest of which is dynamically maintained at value determined by a user-supplied dc reference input, and all other outputs assume values in proportion to their ratios at the input.

Amplitude normalization is a pervasive requirement in signal analysis, estimation, and pattern recognition. This is performed on a one-dimensional signal by automatic gain control, which maintains some measure of the signal (say, its rms or peak value) at a prescribed level. We are interested here in signals which occur in parallel arrays, such as the outputs of multiple sensors. The information in these cases resides *not in the absolute magnitudes* of individual components of the set (which often have a very wide dynamic range) but solely in the *ratios between these components*.

Analysis of such signals usually begins by multiplexing each channel into an A/ D converter and performing normalization using serial digital techniques, prior to extraction of specific features (Fig. 1). This entails finding the largest signal in the set at a given sample instant and dividing all signals by this value. One of the channels will thus be maintained at a controlled value while the remainder assume values proportional to their ratios in the input array.

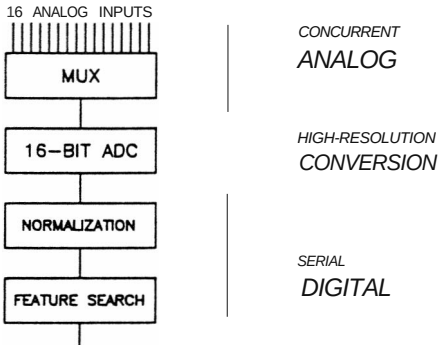

Fig. 1. A typical pattern recognition scheme using a high-resolution *A/ D* converter.

This method has disadvantages. First, it requires the use of an A/ D converter having *much greater resolution* than the information content. In speech recognition, for example, feature extraction can be performed with good accuracy on the normalized power spectrum in 16 frequency bands quantized to 32 amplitude levels (5 bits). On the other hand, the dynamic range of the "raw" spectrum may vary over 50-60 dB (a further 9 bits), requiring a total resolution of at least 14 bits. AGC can sometimes be applied to speech input prior to separation into frequency channels, allowing the use of a low-cost 8 bit A/ D converter. In a true *multichannel* situation AGC cannot be applied to each channel independently, as this would destroy the ratio information. It will be apparent, though, that the array normalizer described here does perform a kind of "space-domain" (rather than time-domain) AGC.

Second, considerable time is required for serial normalization, even using optimized binary routines; this problem will be worsened by the slower conversion time of a high-resolution converter. When the information bandwidth is low and relatively few channels need to be serviced, this may be tolerable, but in cases where high bandwidth is essential and/ or there are a very large number of channels, serial normalization may be impractical. The circuit described here operates essentially instantaneously, that is, all the output voltages respond to any input voltage changes, from a single channel to the entire set, typically within 1 μs.

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Fig. 2 shows how this concept is utilized. The parallel inputs are applied directly to the array normalizer; its outputs are multiplexed into a low-resolution *AI D* converter. The normalizer ensures that at least one of the output channels is equal to the full-scale range of *AI D* converter, so its output can be subjected immediately to a digital feature-search process with the full resolution always utilized.

We first consider a basic circuit capable of concurrent normalization of *N* inputs in the form of currents, having inherently fast response. A limitation of this mode is that the peak output may still vary over output an *N:* 1 range. The addition of a closed-loop control system which overcomes this limitation is then described. It allows the user to supply a reference voltage input to which value the largest output is maintained. However, the settling time of this loop can be as long as 10 μs under worst-case input conditions.

Next, the complete monolithic circuit, which can operate from supply voltages as low as ±3 V with a quiescent dissipation of less than 1 mW, is described in detail, with a discussion of various sources of error. Finally, measurements of static accuracy and dynamic behavior are presented.

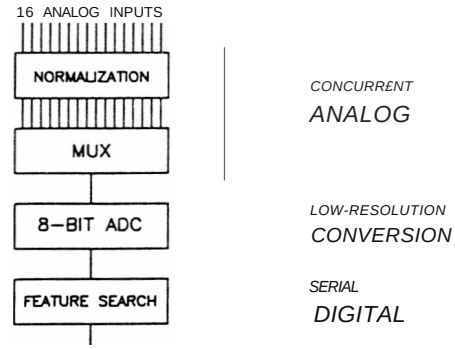


Fig. 2. An alternative scheme using an analog array normalizer and low-resolution converter.

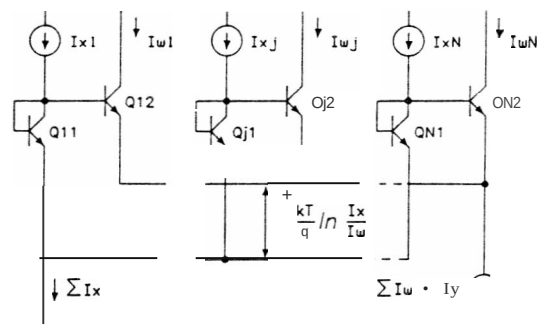


Fig. 3. The basic normalizer circuil: inputs are I_x and outputs are I_w. All transistors are assumed to have the same emitter area.

BASIC CIRCUIT DEVELOPMENT

Translinear Array Normalizer

Fig. 3 shows a basic normalizing circuit [1], [2] having *N* analog inout currents *Ix)* and output currents I_{wJ}. If the transistors are ideal, in particular, having an exactly logarithmic relationship between the emitter-base voltage and collector current, and all transistors have the same emitter saturation current *Is,* it will be at once apparent that the voltage appearing between the common emitter nodes must be

$$V = \frac{kT}{q}\ln\frac{I_{xj}}{I_s} - \frac{kT}{q}\ln\frac{I_{wj}}{I_s} = \frac{kT}{q}\ln\frac{I_{xj}}{I_{wj}} \qquad (1)$$

where $1 < j < N$. This voltage is the same for all transistors pairs, thus forcing all the ratios to be equal:

$$\frac{I_{x1}}{I_{w1}} = \frac{I_{x2}}{I_{w2}} \cdots = \frac{I_{xj}}{I_{wj}} \cdots = \frac{I_{xN}}{I_{wj}} \qquad (2)$$

Simultaneously, the sum of all the outputs must be equal to the source current *Iv* (alphas are assumed to be unity). Since the inputs are independent, the outputs have to adopt values which "solve" this set of equations dynamically. Noting that

$$\frac{\sum(I_{xj})}{\sum(I_{wj})} = \frac{I_{xj}}{I_{wj}}$$

and

$$\sum(I_{wj}) = I_y$$

the solution is

$$I_{wj} = I_y\frac{I_{xj}}{\sum(I_{xj})}, \qquad (3)$$

that is, each element in the output array is equal to the corresponding element in the input array, divided by the sum of all the inputs and scaled by the current *Iv* (which, in practice, will be proportional to an externally controllable multiplying input voltage V_y).

This can alternatively be expressed as

$$V_{wj} = V_y\frac{V_{xj}}{\text{ave}(V_{xj})} \qquad (4)$$

where $V_{x)}$ and $V_{w)}$ are the external interface voltages proportional to *Ix)* and *Iwi'* respectively, and the scaling of *V''* includes the factor *N.* It is important to realize that the response time of all the outputs to a change in any number of the inputs is essentially instantaneous, determined only by the current-mode bandwidth of the transistors. This remains basically true for an array of any size. *The array-normalizer provides an excel/ent example of the power of analog circuits to perform truly concurrent signal processing.*

Peak Tracking Mode

There is a fundamental weakness with the processor at this stage of development, arising directly out of the function shown above. For a given input level for one or more

signals, the average of the inputs can vary over a range of *N:* 1, depending on whether all inputs are present or only a single input is present. In other words, there is a *pattern sensitivity* which can result in an *N :* 1 variation of output level. This amounts to a loss of 4 bits of resolution when an *AI D* is used to process the output of the 16-channel normalizer. It would be better to arrange matters so that at least one output is maintained at some preset level, supplied by the user and conveniently equal to the full-scale range of the *AI D* converter (or other following process).

To do this, the voltage outputs V_{wj} are compared to a reference input V_w, using a peak-seeking control loop (described below) which dynamically adjusts the current *Iv* until the largest output just equals that reference, that is, '

$$V_{wj} = V_w \frac{V_{xj}}{\max(V_{xj})}. \tag{5}$$

In principle, this loop needs no "memory," since tracking of $\max(V_{xj})$ is continuous, but in practice a capacitor is required to stabilize the control loop.

IMPLEMENTAnON

The choice of 16 channels was made early in the development, this being suitable for speech-recognition work and also realistic from the point of view of packaging. By bringing the emitter nodes out to pins, it is possible to expand to any number of channels, since the full array of inputs and outputs would still be constrained by (2). To maintain accuracy it is important that the thermal voltage kT/q be the same for all packages, requiring a low quiescent operating power and the use of modest current levels for the signals. Temperature differentials must also be minimized by ensuring that the circuit can operate from the lowest possible supply voltages; ±3 V seemed a reasonable goal. The signal voltages, however, should be able to exceed the supplies; this is especially important for the inputs.

It was appropriate in this development to work toward a low-cost chip, and not utilize advanced technology, such as compatible FETI bipolar transistors, thin-film resistors, and laser-trimming. Thus, the circuit was designed using a standard junction-isolated bipolar process with diffused resistors. A nitride capacitor, used to HF stabilize the peak-tracking loop, was the only departure from standard processing.

Simple circuit techniques were used to realize the input and output voltage-mode interfaces, since the cell design had to be amenable to layout in array form. Likewise, the peak-tracking loop was implemented using relatively sparse means. In so doing, some conscious concessions to accuracy had to be made; the source of these errors, and methods to eliminate them, are discussed below.

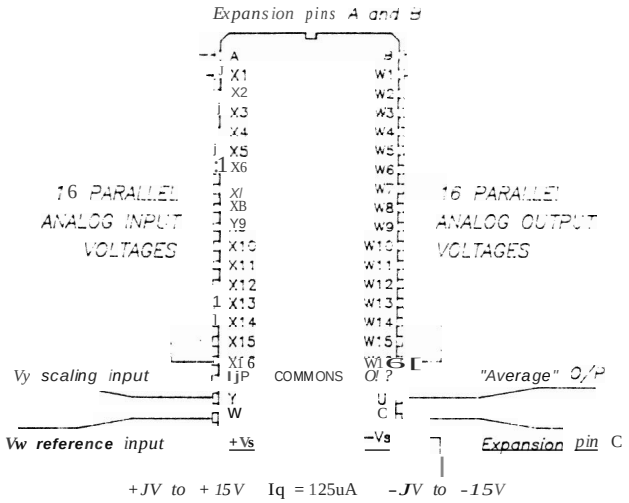


Fig. 4, General package organization.

General Development

The integrated circuit provides voltage-mode interfaces for inputs and outputs. Package pins 2-17 are used for inputs and the opposing pins 25-41 are used for outputs (see Fig. 4). Inputs are positive-going from an analog common; since the normalizer (using n-p-n transistors) requires positive input currents, this can be achieved using an op-amp to force the collector current and establish a high-quality virtual-ground at which the input is converted to a current using a series resistor, as shown in the simplified schematic of the complete processor, Fig. 5.

Input currents in all the transistors Q_{ji} ($1 \leqslant j \leqslant 16$) are collected at the input of current-mirror Q171 - Q174' which places the emitter-base nodes of the core transistors near to $-V_s$. The mirror has a reduction ratio of 16 : 1, so that the output *U* corresponds to the average of the input currents. This output provides an extra degree of flexibility to the device, and is useful as a monitor of the total signal level.

Ideally, current-to-voltage conversion would also be performed by an op-amp with the load resistor in the feedback path. This would provide a buffered output with the same polarity as the input, and also ensure that Q_{j_1} and Q_{j_2} operate at equal *Vee'* important if the full accuracy of the translinear cell is to be realized. However. this complexity could not be afforded, and simple collector load resistors were used. The separate common node may optionally be grounded, since the collectors of output transistors Q_{j_2} can be biased down nearly to $-V_s$. The resulting sign inversion between inputs and outputs can usually be tolerated; buffering and inversion can be provided after output multiplexing.

The emitter supply current (*Iv* in Fig. 3) is provided in one of two ways. To implement the mode embodied in (4), an input V_V is applied to pin 19. For $V_V = 1\ V$ the current in Q181 is 50 μA. Q182 has an emitter area 16 times that of Q_{181}, so I_y = 800 μA. When all inputs V_x *) are equal, I_y divides equally into 16 components of 50 μA and outputs

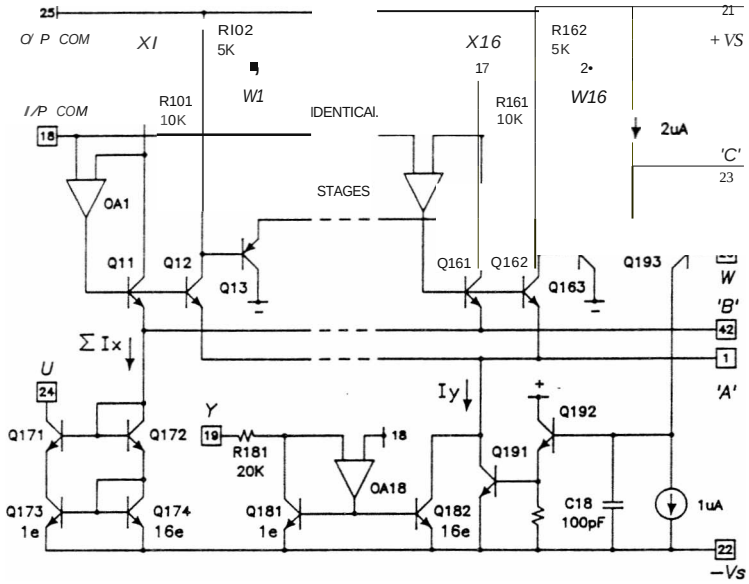


Fig. 5. Main elements of the complete circuit.

$V_w(*)$ are 250 mV below the output common node; when only one input has significant value, the full 800 μA flows in just one output transistor, and the corresponding output voltage is then 4 V below output common. It will be apparent that the scaling is exactly unity when four of the 16 inputs are equal and the remainder are zero, a design choice based on some assumptions about the statistics of typical patterns. (Note that this scaling differs from (4) by a factor of 4.)

The peak-tracking mode is somewhat easier to use, since it ensures that the largest output is always accurately equal to the reference voltage V_w which is typically - 1 to - 2.5 V. In this mode, the V_Y input is not used; I_V is now supplied by Q_{191}, which is controlled by the voltage at the base of Q192. When none of the outputs is sufficiently negative to turn on any of the peak-detectors Q_{j_3} ($1 \leqslant j \leqslant 16$). CIS charges positively, increasing I_v until one of the peak-detectors (which are high-gain vertical-lateral p-n-p transistors) turns on sufficiently to leave just 1 μA in Q_{193} (a lateral p-n-p of similar emitter area). Since the emitter current of the (usually single) peak-detecting transistor is also 1 μA, the peak output voltage in the array $V_w(*)$ is within a few millivolts of V_w. The exact value of the offset is unimportant, since the objective is simply to ensure that one or more of the outputs is reasonably close to the full-scale voltage. If two inputs are at exactly the same value. there will be an output deficit of 18 mY. Rarely in practice will all inputs be exactly equal; in such a case the deficit could be as large as $Vt \cdot ln(16)$ or 72 mY, but even this is less than 3 percent of a typical - 2.5 V full-scale output.

In applications where it is desirable to interface directly to an A/D converter having an input range of 0 to + 2.5 V, the reference input can be grounded ($V_w = 0$) and the output common (pin 25) taken to + 2.5 V. This results in zero-scale and full-scale being transposed; thus, the digital output is in two's-complement form.

CIS provides the dominant pole for HF compensation of the control loop. The time constant it forms with the gm of Q_{J_3}/Q_{193} is modified by the voltage gain from the base of Q_{192} to an output; the gain calculation must take into account both the variation of the gm of Q_{191} as I_y varies and the effect of this current dividing into the devices, Q_{J2}. The net result is a small-signal response time which is essentially independent of the input pattern, and typically 500 ns.

The large-signal response time to the normalizer is affected by the tracking loop behavior only when a change in input pattern occurs, requiring I_y to change: the resulting change in the V_{be} of Q_{191} requires CIS to charge through a voltage step. The worst case occurs when the pattern changes from a "single-input" situation to an "all-equal" one; then I_V must change by a ratio of 16: 1, resulting in a step of about 72 mV at 300 K. The ohmic emitter resistance of Q191 raises this to about 100 mY, resulting in a worst-case slewing time of 100 pF · 100 mV/ 1 μA, or 10 μs.

Cell Design

The basic cell. comprising the core transistors $Q_{J,}$ and Q_{J_2}, the peak detectors Q_{j_3}, and the op-amps OA), is shown on the right of Fig. 6. Clearly, it would not be practical to use 16 fully independent op-amps. Instead, a shared biasing scheme, shown on the left side of the figure, provides a bias line for the bases of transistors Q_{J4} such that their emitters are within a millivolt or two of input common and the emitter node behaves like a virtual ground. An emitter bias of 2 μA is provided by Q_{J_5}, and then removed in the collector circuit by $Q_{J6;}$ these transistors are biased by additional circuitry not shown in the figure. Thus, all of the

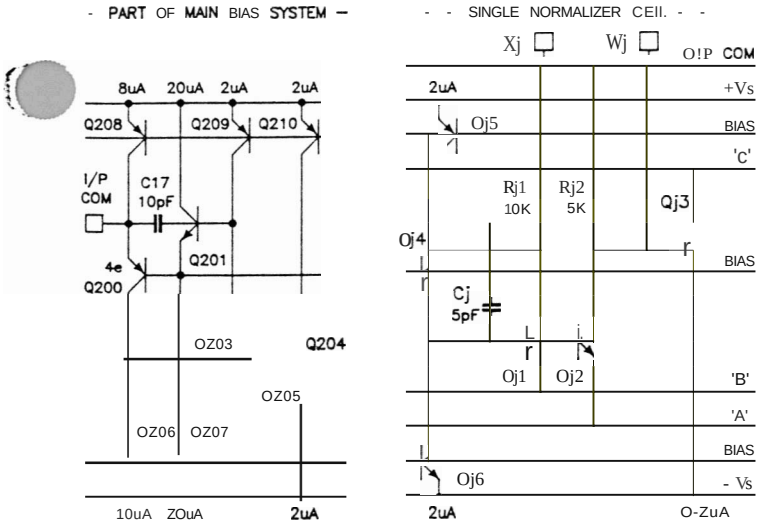


Fig. 6. Details of the cell design and shared bias circuitry.

current generated by the input V_{xj} through the 10 kΩ resistor R_j, is forced to flow in Q_{j_1}.

Errors at Small Inputs

The net input offset voltage is determined by the current-density ratio between Q_j and Q200 in the common bias circuit, plus a component due to the imbalance between the upper and lower 2 μA current sources which effectively flows in R_j. Assuming a 10 percent mismatch in 2 μA, the latter amounts to 1.25 mV. The large area covered by the normalizer cells will inevitably result in a gradient of offset voltage across the 16 stages. In the absence of trimming, this offset scatter sets the lower limit to the dynamic range.

Q_j provides the necessary virtual-ground, but it does not provide any current gain to the bases of Q_{jt} and $Q_{h'}$ as implied by the simplified schematic of Fig. 5. Thus, the signal must provide not only the base current of Q_{j_1}, which is a constant, small fraction of the signal, but also that of Q_{J2}" which is determined by the output bias. A complete understanding of the consequences of this requires a careful consideration of the whole system under different operating conditions and for a variety of input patterns and absolute levels. But some trends can be pointed out here.

First, note that if the betas of Q_h are not significantly dependent on collector current (true of most modern, clean processes), the fractional loss of signal current to their bases remains *in proportion* to the output currents; input devices Q_j, therefore continue to operate with the same set of ratios, right down to the point where *all* of the signal current is used as base drive to devices Q_{j_2}. Down to this breakpoint the finite beta of Q_{j_2} is troublesome only to the extent that it introduces a small gain error from emitter to collector. This is compensated in the design of the V_y terface to minimize errors in the averaging mode. When used in the peak-tracking mode, the error is eliminated by the closed-loop nature of the system.

Errors at High Inputs

At high input levels, two effects impact accuracy. The first is minor; as the base currents in Q_j, and Q_{j_2} become comparable with the 2 μA bias current, the V_{be} of Q_{J_1} rises and the summing node is no longer at the input common voltage. For a full-scale input of $V_{xj} = +15$ V, when $I_{ej} = 1.5$ rnA and I_{bj} would typically be 5 μA, the change in the summing node voltage is about $Vt \cdot \ln(5/2)$ or 24 inv, resulting in a gain error of about 0.16 percent (with a peak nonlinearity of about 0.07 percent) for this channel considered in isolation. Note, however, that a gain error is not of itself a problem, to the extent that all inputs are equally affected, and the ratios are unchanged. The effective nonlinearity is likewise reduced when the system is considered as a whole.

The ohmic resistance R_e in the emitters of the core transistors (due largely to *rbb'*) is more troublesome, since it can seriously impair the logarithmic behavior of the junctions and, thus, destroy the exactness of the ratiometric relationship shown in (2). It is not difficult to include R_e into the original equation, provided that the voltages $I_{xj}R_e$ and $I_{wj}R_e$ are small. (It is assumed for simplicity that all the core transistors have the same R_e.) Equation (1) becomes

$$V = \frac{kT}{q} \ln \frac{I_{xj}}{I_S} + I_{xj}R_e - \frac{kT}{q} \ln \frac{I_{wj}}{I_S} - I_{wj}R_e \qquad (6)$$

which can be expanded to

$$V = V_T \ln \frac{I_{xj}}{I_{wj}} \cdot \frac{(1 + I_{xj}/I_r)}{(1 + I_{wj}/I_r)} \qquad (7)$$

where $I_r = kT/qR_e$, provided that $I_{xj}R_e$ are less than about $0.1kT/q$.

Thus, (2) becomes

$$\frac{I_{x_1}(1 + I_{x_1}/I_r)}{I_{w_1}(1 + I_{w_1}/I_r)} \quad \frac{I_{xj}(1 + I_{xj}/I_r)}{I_{wj}(1 + I_{wj}/I_r)} \quad \frac{I_{xN}(1 + I_{xN}/I_r)}{I_{wN}(1 + I_{wN}/I_r)}. \qquad (8)$$

A general solution for $I_w(*)$ does not exist, but some observations can be made. First, in the special case where the total input current ΣI_{xj} is equal to the total output current ΣI_{wj}, the inputs and output ratios will be identical. Second, when the input currents are large, the numerator term in (8) dominates and the errors will be approximately parabolic. Intuitively, we would expect parabolic errors of opposite polarity to occur when the inputs are small.

SPICE was used to investigate these errors numerically. The simulation used a core of 16 channels having transistors which were ideal except for the inclusion of emitter

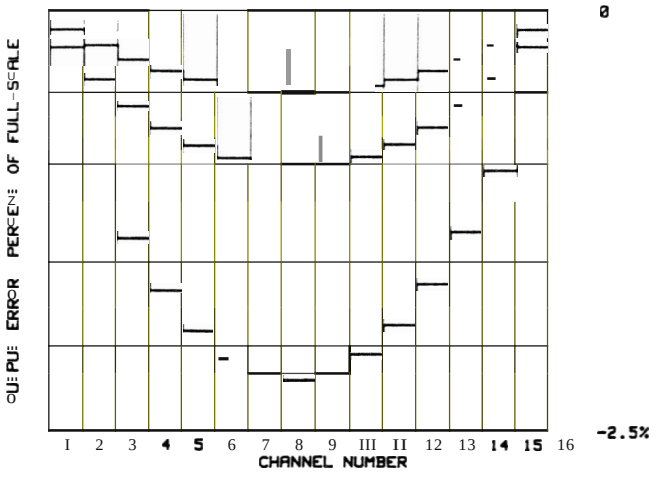


Fig. 7. Theoretical errors for ohmic emitter resistance of I, 2, and 5Ω (top to bottom, respectively) and maximum V_w of + 10 V.

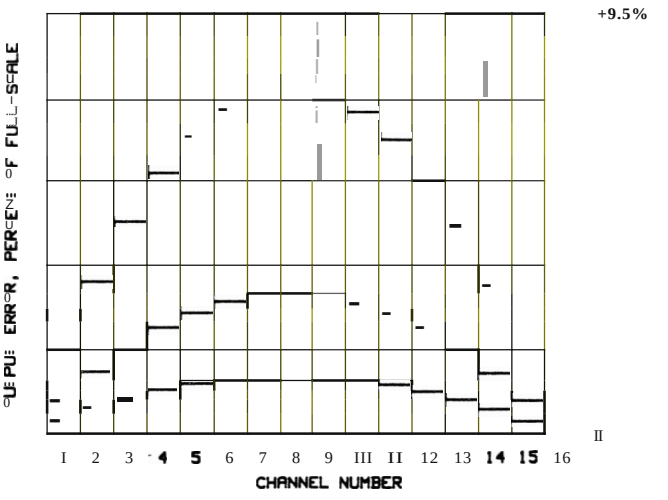


Fig. 8. Theoretical errors due to finite Early voltage of 150 V, with peak outputs of 2.5, 1 and 0.4 V (top to bottom, respectively).

resistance. The inputs increased linearly with channel number, from 62.5 μA for channel 1 to 1 rnA for channel 16, corresponding to apeak input of + 10 V in the complete circuit. The output current I_y was maintained at the level required to generate 500 μA in the output of channel 16, corresponding to the use of the peak-tracking mode with V_w = -2.5 V.

Fig. 7 plots the error versus channel number for R_e = 1, 2, and 5 Ω. The core transistors in the monolithic design are such that an R_e of less than 2 Ω is predicted. Consequently, errors due to R_e should be below 1 percent for peak inputs of + 10 V.

Finally, a small additional error is caused by the finite Early voltage of the output transistors Q_{j_2}. An analytic approach shows that this error arises only from *differences* in collector voltages, apart from the minor variation of alpha with supply voltage (which effect is eliminated using the peak-tracking mode). However, the analysis results in an implicit solution, similar in form to (8), and SPICE was gain used to explore the effect. The input conditions were the same as before, but the transistors were now ideal except for BF = 300 and VAF = 150, arid I_y was adjusted for peak outputs of - 400 mV, -1 V, arid - 2.5 V. As before, the error was calculated as a percentage of the full-scale output and plotted versus channel number (Fig. 8). Under the worst probable conditions the peak error is under 0.5 percent. Cascodes could be added to eliminate this source of error.

MONOLITHIC EVALUATION

Fig. 9 is a photomicrograph of the monolithic prototype. The array is on the left-hand side, with inputs along the bottom and outputs along the top. The rest of the chip area is taken up with the biasing system and the peak-tracking loop, a prominent feature of which is the 100 pF stabilizing capacitor.

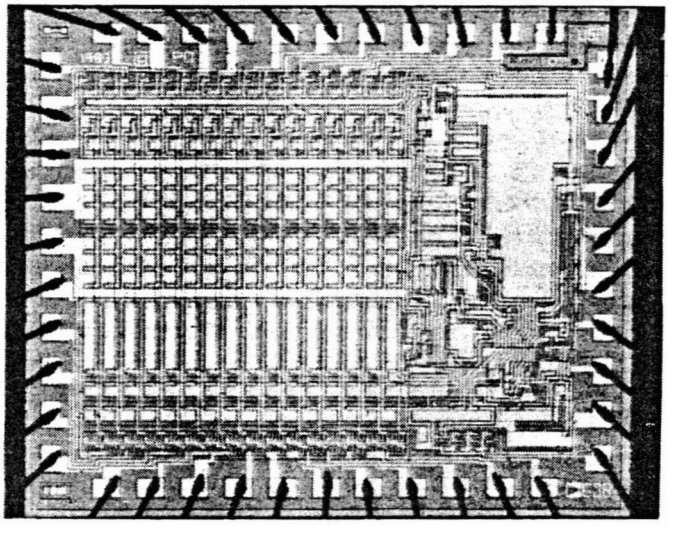
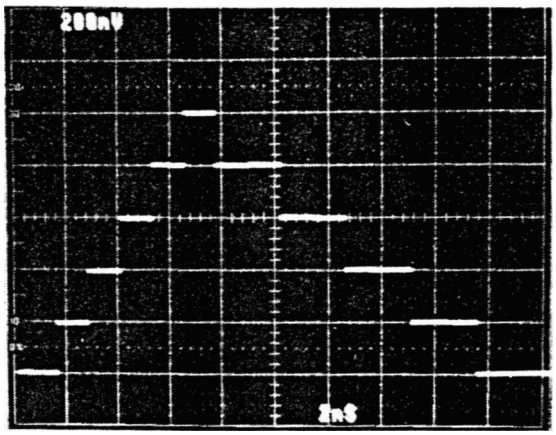


Fig. 9. Photomicrograph of the analog array processor. Chip size is 135 X 115 mils.

Static Performance

Evaluation was carried out in most cases using the peak-tracking mode, with supply voltages of ±5 V. The inputs were voltages having fixed ratios but variable absolute magnitude. In Fig. 10(a), inputs of 0 were applied to CH 1, 15, and 16; +2 V to CH 2, 13, and 14; +4 V to CH 3, 11, and 12; +6 V to CH 4, 9, and 10; +8 V to CH 5, 7, and 8; + 10 V to CH 6. V_w was -1 V. The outputs were displayed using a specially constructed plug-in unit for a Tektronix 7000-series oscilloscope, which divides each sweep into 16 zones, each corresponding to a channel. An optional sign-inversion can be introduced, and this was used in preparing the traces shown here. The outputs are visibly close to their exact values. In Fig. 10(b), exactly the same pattern was applied. but with the maximum peak input reduced to + 10 mY; V_w was maintained at -1 V. Each major vertical graticule division now corresponds to 2 mV referred to the input, and the input offsets are clearly



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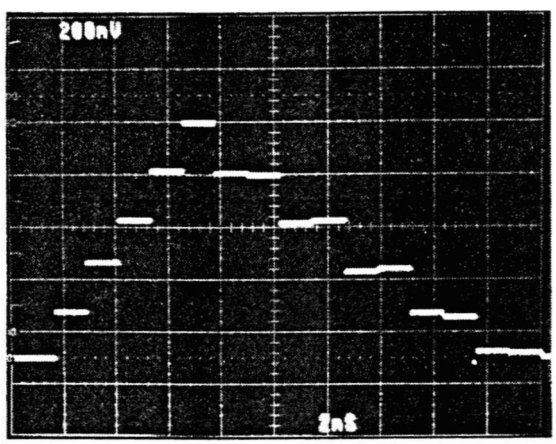

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Fig. 10. (a) Outputs of CH 1-16 displayed from left to right. Peak input is + 10 V (see text). (b) Array output with same *ratios* as in Fig. 10(a). but peak input of only + 10 mY.

in evidence. Separate measurements show an offset scatter of about ±1 mV on the better parts, with some evidence of a systematic bowing toward the center of the array.

Fig. 11 illustrates this normalizing response using a 1 kHz triangle wave of + 100 mV to + 10 V as the input to CH 6, with the other inputs remaining in the ratios stated above. This demonstrates the ability of the processor to reject relatively fast change of 100 : 1 in the magnitudes of the inputs while preserving the pattern in the output. The peak error can be estimated as about 3 percent. More exact evaluation of the static behavior was carried out using an instrumentation system consisting of two Data Precision type 8200 calibrators, an HP3456A multimeter, and an HP3488A multiplexer, controlled by an HP9836 computer. This scheme provides inputs of $V_{pk}/16$ to V_{pk} in increments of $V_{pk}/16$, where V_{pk} can be programmed from 0 to + 20 V; V_w can be varied from 0 to - 5 V. Using this system, the peak errors for $V_{pk} < 2$ V remain less than 1 percent, but deteriorate significantly at inputs of $V_{pk} \geqslant 10$ V. The sign of the error is opposite to that expected, on the assumption that it is entirely due to the emitter resistance of input transistors, and a satisfactory explanation of this "excess" error has not yet been found.

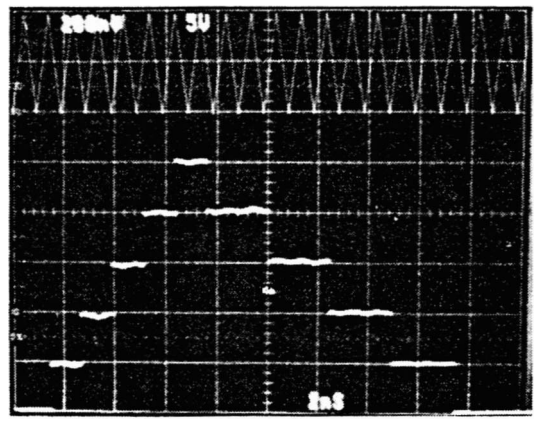

Fig. 11. Output array (lower trace) for same ratios as Fig. 10. but peak input dynamically swept for + 100 mV to + 10 V (top trace).

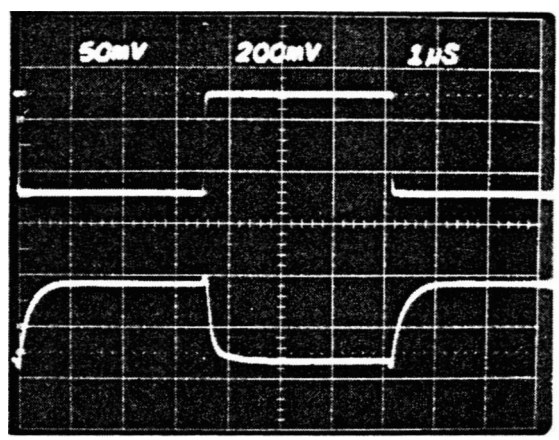

Fig. 12. Dynamic behavior; see text for details.

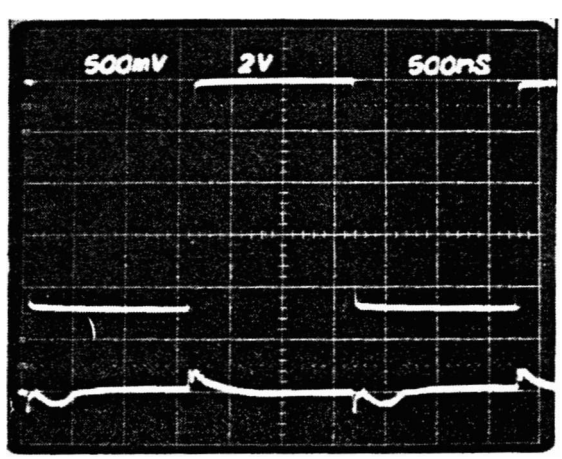

Fig. 13. Dynamic behavior using peak-tracking loop (see Iext).

Dynamic Performance

Complete evaluation of the processor under dynamic conditions is a challenge, since there obviously are limitless possible combinations of 16 signal inputs and two control inputs. The results presented here serve to demonstrate in a

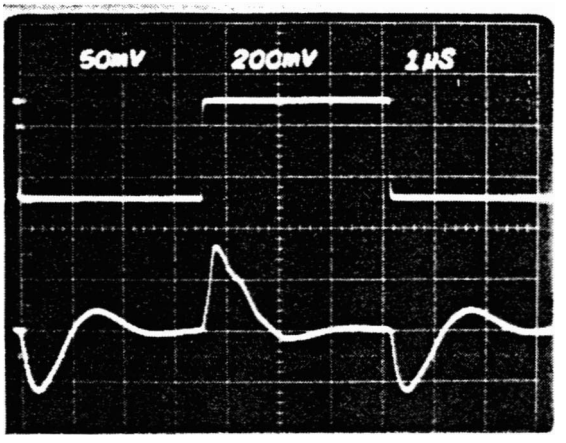

Fig. 14. Dynamic behavior (see text).

general way that the device is inherently capable of sub-microsecond concurrent processing.

In Fig. 12, the input to CH I, shown as the top trace, was switched from +900 mV to +1.3 V. wh.ile all other channels were held at +0.75 V. An external input of VI' = +10 V was used; the peak-tracking feature was disabled in this case. The theoretical CH 1 outputs levels are

$$-\frac{10\text{ V}}{4}\cdot\frac{0.9}{0.9+15\times0.75} = -0.185\text{ V}$$

when CH 1 = 0.9 V

and

$$\frac{-10\text{ V}}{4}\cdot\frac{1.3}{1.3+15\times0.75} = -0.259\text{ V}$$

when CH 1 = 1.3 V.

The lower trace shows that the 74 mV CH 1 output transition occurs within much less than 1 μs.

In Fig. 13, the peak-tracking mode was used (V" = 0, V_w = - 2.5 V). In this case, the input to CH 1 was switched between +1 and +10 V wh.ile all other channels were held at 0. Thus, CH 1 is always the largest input, and the output should remain at −2.5 V. The photo shows a transient error of about ±0.2 V, of about 700 ns in duration. In this case, the total emitter supply current (I_y) does not have to vary. so the response time of the tracking loop is not a major factor in determining the overall response. However, in Fig. 14, CH 2-15 were varied between +0.9 and +1.3 V while CH 1 was held at +10 V; the lower trace shows the CH 1 output. The current II' now has to adapt to the input conditions, and a slew-rate-limited effect is visible as the voltage on CI8 varies.

CONCLUSION

The basic concept of an analog array normalizer has been presented and the design and performance of a practical monolithic implementation described. This circuit was developed primarily to investigate the feasibility of the concept, and has not yet been evaluated in an application. On the basis of th.is work, it is apparent that additional sources of static error need to be identified. It also seems likely that a slightly more complex cell design may be necessary. While the scatter on input offset voltages is tolerable, a significant extension of the dynamic range could be achieved by laser trimming the offsets.

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